Jun Yang

Electrical and Computer Engineering
University of Pittsburgh
1111 Benedum Hall
Pittsburgh, PA 15261

Work Phone: (412) 624-9088
FAX: (412) 624-8003
Email: juy9@pitt.edu

RESEARCH INTERESTS

Processor microarchitecture:	chip multiprocessors, interconnection networks, 3D chips, cache management, power and thermal management, performance optimization.
Memory systems:	emerging memory technologies, main memory systems.
Embedded systems:	energy conservation, network processors, sensor networks.
Hardware security:	architecture support for secure software execution.

EDUCATION

Ph.D. in Computer Science, University of Arizona, September 2002; Advisor: Rajiv Gupta
M.S. in Computer Science, University of Pittsburgh, June 1999; Advisor: Rami Melhem
M.A. in Applied Mathematics, Worcester Polytechnic Institute, August 1997; Advisor: Dalin Tang
B.S. in Computer Science, Nanjing University, P. R. China, June 1995.

PROFESSIONAL POSITIONS HELD

Associate Professor, Department of Electrical and Computer Engineering, University of Pittsburgh, September 2009 – present.
Assistant Professor, Department of Electrical and Computer Engineering, University of Pittsburgh, September 2006 – August 2009.
Assistant Professor, Department of Computer Science and Engineering, University of California, Riverside, September 2002 – August 2006.

AWARDS

Best Paper Awards, ISLPED 2013; ICCD, processor architecture track 2007
NSF Faculty Early Career Development Award (CAREER) 2008
Best Paper Nominee, The 15th International Symposium on High-Performance Computer Architecture 2009
International Symposium on Low Power Electronic Design 2012
Regent's Faculty Fellowship / Faculty Development Award, UC Riverside 2003, 2004

EXTERNALLY FUNDED RESEARCH PROPOSALS

National Science Foundation, PI (Co-PI: Bruce Childers, Youtao Zhang), *SHF: Small: A Brick in the Wall: Achieving Yield, Performance and Density Effective DRAM Beyond 22nm Technology,* CCF-1422331, $449,999, 7/15/2014-7/14/2017.

Abstract: For more than four decades, computer main memory has predominantly used Dynamic Random Access Memory (DRAM). Much of DRAM's success is due to continuous shrinking of the silicon devices in the memory, which allows DRAM capacity to double roughly every two years. Yet, this trend is coming to a halt largely due to the inability of the manufacturing process to precisely control the sizes of a device, which is termed process variation (PV). There are some known problems with PV. However, a vital problem that has rarely been investigated in the past is that PV can cause critical memory operational timing violations. Such violations slash DRAM chip yield, and immediately increase the chip cost.

This research aims to address the challenge imposed by PV on DRAM device timing to chip yield. Our key approach is to expose inherit operational timing variations caused by PV, so that they can be managed externally by the memory controller. The impact of this research is to enable the continuous scaling of the DRAM technology to achieve the cost, capacity and performance requirement for future computing in engineering, scientific, biological, environmental, business and consumer applications.

National Science Foundation, PI (Co-PI: Bruce Childers and Youtao Zhang), Research Experience for Undergraduates supplement to *SHF: Small: A Brick in the Wall: Achieving Yield, Performance and Density Effective DRAM Beyond 22nm Technology,* CCF-1422331, $24,000, 7/15/2015-7/14/2017.

National Science Foundation, PI (Co-PI: Rami Melhem)**,** *EAGER: Tackling the Variations and Instability of Nanophotonic Interconnection Network via Architecture Techniques,* CCF-1242657, $130,000, 8/1/2012-7/31/2013.

Abstract: In current designs of computer chips, electrical wires are used for communication between the different components of the chip. As technology scales down, the signal delay and power consumption caused by electrical wires start to dominate the overall delay and power consumption on the chip. A promising alternative is to use optical waveguides for communication. However, many fundamental challenges face the integration of optical devices into commercial chips. The two major challenges addressed in this project are process variations and thermal sensitivity of optical devices. Both lead to their resonance wavelengths drifts, which cause the optical network to lose significant bandwidth. The proposed research takes an architectural approach to endure and tolerate drifts in wavelength resonance. It investigates different techniques to maximize the effective bandwidth at run-time in the presence of defects and changes in operating temperatures. These techniques treat bandwidth as a resource that is allocated, on-demand, to different nodes in a way that masks the resonance shifts of optical devices. Since the aggregated available on-chip bandwidth is usually larger than the instantaneous demand for bandwidth, the effect of the imperfect hardware is mitigated by appropriately assigning wavelengths to nodes, thus offering a reliable and near perfect optical communication layer to the other components of the system.

National Science Foundation, co-PI (PI: Bruce Childers, other co-PIs: Sangyeun Cho, Rami Melhem, Daniel Mossé, Youtao Zhang)**,** *CSR Large: Storage Class Memory Architecture for Energy Efficient Data Centers*, CNS-1012070, $1,912,126, 7/1/2010-6/30/2014.

Abstract: Data centers in the U.S. are poised to consume around 100 billion KW of energy, half of which in servers. The majority of power consumption will shift from the processor to main memory. This project, rather than relying solely on DRAM, uses multiple technologies to construct a high-capacity, energy-efficient memory system for virtualized computer servers with a new Storage Class Memory Architecture that incorporates multiple memory technologies such as DRAM, Phase-change memory (PRAM) and Flash. The fundamental contributions include: a new integrated memory architecture that seamlessly manages hybrid memory resources; novel algorithms and policies for energy, performance and endurance management; better understanding of the hypervisor's role in resource management and its interaction with upper and lower system layers; and a new hybrid DRAM and PRAM main memory controller. This research represents a new "green computing technology" that satisfies the demands of future computing systems (e.g., cloud computing, server farms, commodity computers) in an exceptionally low energy manner.

National Science Foundation, co-PI (PI: Bruce Childers, other co-PIs: Sangyeun Cho, Rami Melhem, Daniel Mossé, Youtao Zhang)**,** Research Experience for Undergraduates supplement to *CSR Large: Storage Class Memory Architecture for Energy Efficient Data Centers*, CNS-1012070, $16,000, 2013.

Intel Corporation, PI, *Towards Low-Power System-on-Chip,* $50,000, November, 2008 – October, 2009.

Abstract: A system-on-chip (SoC) may contain combinations of cores of different functions such as microprocessors, memories, a/v controllers, modem, 2D and 3D graphics controllers, DSP functions etc. The high integration of vastly different function cores on-chip with the continuous technology shrinking brings forth the challenges in low power SoC designs. SoCs are widely used in consumer electronics, mobile internet devices, and embedded markets. Most of them are battery powered. An energy-efficient design can not only extends the battery life, but also allow for higher performance and higher integra-

tion of more IP blocks on-chip. In this proposal, we put forward a suite of techniques to tackle the critical factors of the power consumption of an SoC, namely the switching activity of different IP blocks, the voltage and frequency of them, and the leakage power of the memory modules.

National Science Foundation, PI, *CAREER: Thermal-Aware Task Scheduling for Embedded Planar and 3D Chip Multiprocessors*, CNS-0747242, $400,000, 9/1/2008-8/31/2013.

Abstract: This CAREER project proposes innovative solutions to tackle the thermal problems for modern compact embedded systems including 2D or 3D multicore processors that support powerful and versatile applications. The objective of this proposal is to develop proactive thermal management techniques which prevent the temperature from increasing above the threshold and avoid performance throttling. This is in contrast to traditional techniques which only react to thermal violations by enforcing performance throttling to cool down the processor. The proposed techniques leverage the natural discrepancies in thermal behavior among different applications, and schedule them among multiple cores to keep the chip temperature within a given budget. The mission of such scheduling is to minimize thermal violations across all cores on-chip, improve the performance, and diminish overheating-induced problems such as reduced reliability, low circuit speed, and high leakage power.

National Science Foundation, PI (Co-PI: Youtao Zhang), *An Update-Conscious Compilation Framework for Energy-Efficient Code Dissemination in Wireless Sensor Networks*, CNS-0720595, $120,000, 9/1/2007-8/31/2009.

Abstract: Wireless sensor networks (WSN) often require code changes, such as software patches, new functions etc. A naïve way of performing code changes in a WSN is to send the code or code differences in form of data packets, and let the sensor nodes compute the new code. Since energy consumed by data transmission is much higher than that consumed by local instruction execution, it is important to be energy-efficient during the code dissemination in WSNs. This project proposes update-conscious compilation for achieving energy-efficient code dissemination. The integrated compilation framework consists of a set of sink-side update-aware compilation techniques, and a sensor-side software-decoder/binary-rewriter. Specifically, the intellectual merits of this project are: 1) update-aware register allocation techniques; 2) update-aware data allocation techniques; 3) update-aware code placement techniques; 4) tools for enabling update-aware compilation. Through this research, we are committed to cultivating a strong interest and a positive attitude among students towards embedded software development.

National Science Foundation, PI (Co-PIs: Sheldon Tan, Jie Chen), *Fast Software Thermal Sensing and Control for Efficient Dynamic Thermal Management*, CCF-0734339, $275,000, 4/1/2006-3/31/2009.

Abstract: This proposal addresses the fundamental challenges in todays on-chip thermal sensing and control problems. The thermal sensing technique in even the most recent processors predominantly relies on thermal diodes or sensors. Both suffer from the fixed-location problem as on-chip hot spots migrate at run time. This project aims to develop novel techniques for spectrum and high precision temperature sensing to mitigate this problem. The proposed solutions can lead to more efficient and effective on-line thermal management. The intellectual merit of the project includes the development of a fast, lean, and accurate software thermal sensor for online temperature tracking. The software adopts a highly efficient and fine-tuned numerical method to calculate temperatures at a fine granularity both temporally and spatially. Experimentation will demonstrate its superior accuracy and speed, and hence the great potential of becoming a truly competitive remedy for chip temperature sensing.

National Science Foundation, PI (PI of collaboration institute: Youtao Zhang), *Collaborative Research: Architectural Support for Security and Privacy Protection on Uni- and Multi- Processors*, CCF-0430021, $80,001 (UCR funds: $54,001), 11/1/2004-10/31/2006.

Abstract: Software programs executing on a broad range of internet systems are constantly subject to malicious attacks in various forms. Program execution behavior might be altered causing substantial damage, data may become corrupted and privacy can be greatly compromised. This proposal develops

a secure processor model which secure applications can easily be built on. We augment the existing microprocessor architecture to incorporate new features. The proposed architectural components address a broad range of attacks on uniprocessor and multiprocessor architectures. In particular, we develop novel architecture support for enhancing uniprocessor security. The confidentiality and integrity of such a microarchitecture are maintained through encryption and decryption of the code and data transferred across the chip. While the efficiency of encryption has been solved successfully by PIs and others, the computation intensive nature of crypto operations has led the verification of inbound traffic being delayed. This project also designs a strong verification engine with which information leakage of on-chip data is prevented. This was a collaborative project with University of Texas, Dallas. The PI there was Professor Youtao Zhang.

National Science Foundation, Senior Personnel (PI: Laxmi Bhuyan, co-PI: Walid Najjar, Gianfranco Ciardo), *MRI: Acquisition of an Ultra Low-Latency Multiprocessor System with On-Board Hardware Accelerators*, CNS-0619223, $330,000, 8/15/2006-7/31/2008.

Abstract: This project, acquiring an extremely low-latency multiprocessor system with on-board hardware accelerators, develops efficient scalable algorithms and software resource management schemes for individual applications. The cluster is used in support of the following projects. 1) Investigation into scalable hardware and software design for Internet web servers and data centers; 2) Symbolic model checking; 3) Pattern discovery for biological applications; 4) Automatic compilation of high-level code, such as C or Fortran, into RTL VHDL code; 5) Warp processing; and 6) Augmenting existing microarchitecture with security protections ensuring integrity & confidentiality of program execution. The proposed cluster can be partitioned into several subclusters that can work independently and simultaneously on different applications, provides ultra low message passing latency within a sub-cluster and between sub-clusters, and provides an SMP environment with processors that can be used for tightly-coupled codes; thus a hybrid programming model suits different applications. The research projects on FPGA compilation, hardware/software partitioning, and CPU micro architecture design require an FPGA-based system for a test bed.

STUDENT ADVISING

GRADUATED PH.D. STUDENTS

1. Yan Luo
   Ph.D. in Computer Science and Engineering, 2005, University of California Riverside
   Performance Evaluation and Low Power Design of Network Processors
   co-advised with Laxmi Bhuyan (UC Riverside) Jan. 2003 – Aug. 2005
   Source of support: NSF grants and TAship
   First employment: Assistant Professor, University of Massachusetts Lowell, MA.
2. Lingling Jin
   Ph.D. in Computer Science and Engineering, 2006, University of California Riverside
   Software Thermal Monitoring and Management for High-Performance Microprocessors
   Major advisor, Sept. 2002 – Aug. 2006
   Source of support: NSF grants, UCR startup fund, and TAship
   First employment: nVidia Corp., CA.
3. Lan Gao
   Ph.D. in Computer Science and Engineering, 2007, University of California Riverside
   Security Designs for Uni and Multi- Processors
   Major advisor, Sept. 2002 – Aug. 2006; co-advised with Marek Chrobak Sept. 2006 – Aug. 2007
   Source of support: NSF grants, UCR startup fund, and TAship
   First employment: VMware Corp., CA.
4. Jia Yu
   Ph.D. in Computer Science and Engineering, 2007, University of California Riverside
   Architectural and Compiler Optimization for Network Processors

Major advisor, Sept. 2002 – Aug. 2006; co-advised with Laxmi Bhuyan Sept. 2006 – Aug. 2007
Source of support: NSF grants, UCR startup fund and TAship
First employment: VMware Corp., CA.

5. Wei Wu
   Ph.D. in Computer Science and Engineering, 2008, University of California Riverside
   Power/Thermal Modeling and Dynamic Thermal Management for SRAM Structure
   Major advisor, Jan. 2004 – Aug. 2006; co-advised with Sheldon X.-D. Tan Sept. 2006 – Jan. 2008
   Source of support: NSF grants and TAship
   First employment: Intel Corp., Hillsboro, OR.
6. Xiuyi Zhou
   Ph.D. in Electrical and Computer Engineering, 2011, University of Pittsburgh
   Dynamic Thermal Management for Microprocessors Through Task Scheduling
   Major advisor, Sept. 2005 – Dec. 2011;
   Source of support: NSF grants and University of Pittsburgh startup fund
   First employment: Microsoft Seattle, WA.
7. Ping Zhou
   Ph.D. in Computer Engineering, 2011, University of Pittsburgh
   Towards Successful Application of Phase Change Memories: Addressing Challenges From Write Operations
   Major advisor, Jan. 2008 – Apr. 2009; co-advised with Youtao Zhang May 2009 – Dec. 2011
   Source of support: NSF grants and TAship
   First employment: Intel Corp., Chandler AZ.
8. Yi Xu
   Ph.D. in Electrical and Computer Engineering, 2012, University of Pittsburgh
   Towards Reliable Nanophotonic Interconnection Network Designs
   Major advisor: May 2010 – December 2012; co-advised with Youtao Zhang Sept. 2007 – May 2010
   Source of support: NSF grant and TAship
   First employment: AMD Research, Beijing China.
   Now: Assistant Professor, Space Science Institute, Macau University of Science and Technology.
9. Bo Zhao
   Ph.D. in Computer Engineering, December 2013, University of Pittsburgh
   Improving Phase Change Memory (PCM) and Spin-Torque Transfer Magnetic-RAM (STT-MRAM) as Next Generation Memories: A Circuit Perspective
   Major advisor, Sept. 2007 – December 2013
   Source of support: NSF grant and TAship
   First employment: Apple, CA
10. Lin Li
    Ph.D. in Electrical and Computer Engineering, April 2014, University of Pittsburgh
    Improving the Reliability of Microprocessors Under BTI and TDDB Degradations
    Major advisor, Sept. 2007 – December 2013
    Source of support: NSF grant and TAship
    First employment: nVidia, CA
11. Lei Jiang
    Ph.D. in Computer Engineering, December 2014, University of Pittsburgh
    Architectural Techniques for Multi-level Cell Phase Change Memory Based Main Memory
    Major advisor, Sept. 2009-Dec. 2013, co-advised with Youtao Zhang through Dec. 2014

Source of support: NSF grants and TAship
First employment: AMD, TX

GRADUATED M.S. STUDENTS

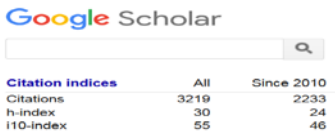
1. Jiannan Wang
   M.S. in Computer Science and Engineering, 2003, University of California Riverside
   An Implementation of Zero Value Based Address Correlation
   Major advisor, Sept. 2002 – Dec. 2003
   Source of support: UCR TAship

CURRENT STUDENTS

1. Jiwei Liu
   Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
   Major advisor, Jan. 2013 – present
   Source of support: NSF grant
2. Rujia Wang
   Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
   Major advisor, Sept. 2013 – present
   Source of support: TAship
3. Wen Wen
   Ph.D. program, Electrical and Computer Engineering Dept., University of Pittsburgh
   Major advisor, Sept. 2014 – present
   Source of support: NSF grants and TAship
4. Xianwei Zhang
   Ph.D. program, Computer Science Dept., University of Pittsburgh
   Co-advisor, Sept. 2013 – present
   Source of support: TAship

REFEREED PUBLICATIONS

The citation statistics are obtained from Google scholar as of December, 2015. The total number of citations for all my publications is 3219. My overall h-index is 30 (at least 30 papers have more than 30 citations).



JOURNALS

[1] Lei Jiang, Bo Zhao, Jun Yang, Youtao Zhang, "Constructing Large and Fast On-Chip Cache for Mobile Processors with Multilevel Cell STT-MRAM Technology", ACM Transactions on Design Automation of Electronic Systems, Vol. 20, No. 4, Article no. 54, pages:54:1-54:24, Sept. 2015, DOI:10.1145/2764903.

[2] Yi Xu, Bo Zhao, Youtao Zhang, Jun Yang, "Simple Virtual Channel Allocation for High-Throughput and High-Frequency On-Chip Routers", ACM Transactions on Parallel Computing, Vol. 2, Iss. 1, Article no. 6, pp. 1-23, May 2015, DOI:10.1145/2742349.

[3] Ping Zhou, Bo Zhao, Youtao Zhang, Jun Yang, "Throughput Enhancement for Phase Change Memories", IEEE Transactions on Computers, Vol. 63, No. 8, pp. 2080-2093, Aug 2014, DOI: 10.1109/TC.2013.76.

[4] Lei Jiang, Yu Du, Bo Zhao, Youtao Zhang, Bruce R. Childers, Jun Yang, "Hardware Assisted Cooperative Integration of Wear-Leveling and Salvaging for Phase Change Memory," ACM Transactions on Architecture and Code Optimization, Vol. 10, Iss. 2, Article No. 7, May 2013, DOI: 10.1145/2459316.2459318.

[5] Bo Zhao, Jun Yang, Youtao Zhang, Yiran Chen, Hai Li, "Common-Source-Line Array: an Area Efficient Memory Architecture for Bipolar Non-Volatile Devices", ACM Transactions on Design Automation of Electronics Systems, Vol. 18, Iss. 4, pages:57:1-57:18, Oct. 2013, DOI:10.1145/2500459.

[6] Bo Zhao, Yu Du, Jun Yang, Youtao Zhang, "Process Variation Aware Non-Uniform Cache Management in a 3D Die Stacked Multicore Processor", IEEE Transactions on Computers, Vol. 62, Iss. 11, pp. 2252-2265, Nov. 2013.

[7] Benjamin C. Lee, Ping Zhou, Engin Ipek, Onur Mutlu, Jun Yang, Youtao Zhang, Bo Zhao, Doug Burger, "Phase Change Technology and the Future of Main Memory," *IEEE Micro*, Vol. 30, No. 1, pp. 131-143, 2010. (acceptance rate = 12/91 = 13%, citations: **141**)

- **IEEE MICRO's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture in 2009.**

[8] Xiuyi Zhou, Jun Yang, Yi Xu, Youtao Zhang, Jianhua Zhao, "Thermal-aware Task Scheduling for 3D Multi-core Processors," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 21, No. 1, pp. 60-71, 2010. (citations: 59)

[9] Xiuyi Zhou, Jun Yang, Marek Chrobak, Youtao Zhang, "Performance-aware Thermal Management via Task Scheduling", ACM Transactions on Architecture and Code Optimization, Vol. 7, No. 1, 2010.

[10] Jun Yang, Lan Gao, Youtao Zhang, Marek Chrobak, Hsien-Hsin S. Lee, "A Low-Cost Memory Remapping Scheme for Address Bus Protection," *Journal of Parallel and Distributed Computing, Elsevier*, Vol. 70, No. 5, pp. 443-457, 2010.

[11] Youtao Zhang, Jun Yang, Hai Vu, Yizhi Wu, "The Design and Evaluation of Interleaved Authentication for Filtering False Reports in Multipath Routing WSNs," *Wireless Networks, The Journal of Mobile Communication, Computation and Information,* Springer Netherlands, DOI: 10.1007/s11276-008-0199-0, Vol 16, No. 1, pp. 125-140, 2010.

[12] Youtao Zhang, Jun Yang, Weijia Li, Linzhang Wang, Lingling Jin, "An Authentication Scheme for Locating Compromised Sensor Nodes in WSNs", Journal of Network and Computer Applications, Vol. 33, No. 1, pp. 50-62, 2010.

[13] Liang Xia, Yongxin Zhu, Jun Yang, Jingwei Ye, Zonghua Gu, "Implementing a Thermal-aware Scheduler in Linux Kernel on a Multi-core Processor", The Computer Journal (Oxford University Press), Vol. 53, No. 7, pp. 895-903, 2010.

[14] Weijia Li, Youtao Zhang, Jun Yang, Jiang Zheng, "Towards Update-Conscious Compilation for Energy-Efficient Code Dissemination in WSNs," *ACM Transactions on Architecture and Code Optimization,* Vol. 6, No. 4, 2009.

[15] Youtao Zhang, Jun Yang, Lan Gao, "Supporting Flexible Streaming Media Protection through Privacy-aware Secure Processors," *Journal of Computers and Electrical Engineering, Elsevier, Special Issue on Circuits and Systems for Real-Time Security and Copyright Protection of Multimedia*, Vol. 35, Iss. 2, pp. 286-299, March 2009.

[16] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, "Energy-Efficient Encoding Techniques for Off-Chip Data Buses," *ACM Transactions on Embedded Computing Systems*, Vol. 8, Iss. 2, Article 9, January 2009.

[17] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, "Tunable and Energy Efficient Bus Encoding Techniques," *IEEE Transactions on Computers*, Vol. 58, No. 8, pp. 1049-1062, 2009.

[18] Wei Wu, Lingling Jin, Jun Yang, Pu Liu, Sheldon X.-D. Tan, "Efficient Power Modeling and Soft-ware Thermal Sensing for Runtime Temperature Monitoring," *ACM Transactions on Design Automation of Electronic Systems*, *Special Issue on Demonstrable Software Systems and Hardware Platforms,* Vol. 12, Iss. 3, Article No. 26 (29 pages), August 2007.

[19] Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Conserving Network Processor Power Consumption by Exploiting Traffic Variability," *ACM Transactions on Architecture and Code Optimization*, Vol. 4, Iss. 1, Article No. 4 (26 pages), March 2007.

[20] Pu Liu, Hang Li, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Fast Thermal Simulation for Runtime Temperature Tracking and Management," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp. 2882-2894, December 2006.

[21] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High-Performance Systems," *ACM Transactions on Architecture and Code Optimization*, Vol. 2, Iss. 1, pp. 34-54, March 2005. (citations: **61**)

[22] Jun Yang, Lan Gao, Youtao Zhang, "Improving Memory Encryption Performance in Secure Processors," *IEEE Transactions on Computers*, Vol. 54, No. 5, pp. 630-340, May 2005 (citations: 72).

- **Featured in MIT Technology Review, July 2005.**

[23] Jun Yang, Jia Yu, Youtao Zhang, "A Low Energy Cache Design for Multimedia Applications Exploiting Set Access Locality," *Journal of Systems Architecture: the EUROMICRO Journal*, Vol. 51, Iss. 10-11, pp.653-664, October/November 2005, Elsevier North-Holland Inc.

[24] Youtao Zhang, Jun Yang, "Reducing I-cache Energy of Multimedia Applications through Low Cost Tag Comparison Elimination," *Journal of Embedded Computing*, Vol. 1, Iss. 4, pp. 461-470, December 2005, IOS Press, Amsterdam, The Netherlands.

[25] Jun Yang, Rajiv Gupta, Chuanjun Zhang, "Frequent Value Encoding for Low Power Data Buses," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 9, Iss. 3, pp. 354-384, July 2004.

[26] Jun Yang, Rajiv Gupta, "Frequent Value Locality and Its Applications," *ACM Transactions on Embedded Computing Systems (inaugural issue)*, Vol. 1, Iss. 1, pp. 79-105, November 2002. (citations: **84**)

[27] Dalin Tang, Jun Yang, "A Free Moving Boundary Model and Boundary Iteration Method for Unsteady Viscous Flow in Stenotic Elastic Tubes," *SIAM Journal on Scientific Computing*, Vol. 21, No. 4, pp. 1370-1386, 2000.

[28] Dalin Tang, Jun Yang, Chun Yang, David N. Ku, "A Nonlinear Axisymmetric Model with Fluid-Wall Interactions for Viscous Flows in Stenotic Elastic Tubes," *Journal of Biomechanical Engineering*, Vol. 121, pp. 494-501, 1999. (citations: **51**)

MAGAZINES AND LETTERS

[29] Zhenning Wang, Jun Yang, Rami Melhem, Bruce Childers, Youtao Zhang, Minyi Guo, "Simultaneous Multikernel: Fine-grained Sharing of GPGPUs", *IEEE Computer Architecture Letters,* 4 pages, September 2015, doi:10.1109/LCA.2015.2477405.

[30] Yan Luo, Jun Yang, Laxmi Bhuyan, Li Zhao, "NePSim: A Network Processor Simulator with Power Evaluation Framework," *IEEE MICRO, Special Issue on Network Processors for Future High-end Systems and Applications*, pp. 34-44, September, 2004. (citations: **62**)

[31] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High-Performance Systems," *IEEE Computer Architecture Letters*, Vol. 2, Iss. 1, 4 pages, September 2003.

CONFERENCE PUBLICATIONS

[1] Rujia Wang, Youtao Zhang, and Jun Yang, "ReadDuo: Constructing Reliable MLC Phase Change Memory through Fast and Robust Readout", *to appear, The 46th Annual IEEE/IFIP International Conference on Dependable System and Networks (DSN)*, Toulouse, France, June 2016.

[2] Xianwei Zhang, Youtao Zhang, Bruce R. Childers, and Jun Yang, "Restore Truncation for Performance Improvement in Future DRAM Systems", ***IEEE the 22nd International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 543-554, March 2016.

[3] Zhenning Wang, Jun Yang, Rami Melhem, Bruce R. Childers, Youtao Zhang, and Minyi Guo, "Simultaneous Multikernel GPU: Multi-tasking Throughput Processors via Fine-Grained Sharing", ***IEEE the 22nd International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 358-369, March 2016.

[4] Jiwei Liu, Jun Yang, and Rami Melhem, "SAWS: Synchronization Aware GPGPU Warp Scheduling for Multiple Independent Warp Schedulers", *to appear,* ***The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)***, pp. 383-394, December 2015.

[5] Xianwei Zhang, Lei Zhao, Youtao Zhang, and Jun Yang, "Exploit Common Source-Line to Construct Energy Efficient Domain Wall Memory based Caches", *The 33rd IEEE International Conference on Computer Design (ICCD)*, New York City, October 2015.

[6] Xianwei Zhang, Youtao Zhang, and Jun Yang, "DLB: Dynamic Lane Borrowing for Improving Bandwidth and Performance in Hybrid Memory Cube", *The 33rd IEEE International Conference on Computer Design (ICCD)*, 8 pages, New York City, October 2015.

[7] Xianwei Zhang, Youtao Zhang, and Jun Yang, "TriState-SET: Proactive SET for Improved Performance of MLC Phase Change Memories", *The 33rd IEEE International Conference on Computer Design (ICCD)*, 7 pages, New York City, October 2015.

[8] Bruce R. Childers, Jun Yang, and Youtao Zhang, "Achieving Yield, Density and Performance Effective DRAM at Extreme Technology Sizes", *International Symposium on Memory Systems (MemSys)*, pp. 78-84, October 2015. DOI: 10.1145/2818950.2818963

[9] Rujia Wang, Lei Jiang, Youtao Zhang, and Jun Yang, "SD-PCM: Constructing Reliable Super Dense Phase Change Memory under Write Disturbance", ***The 20th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)***, pp. 19-31, March 2015. DOI: 10.1145/2694344.2694352

[10] Rujia Wang, Lei Jiang, Youtao Zhang, Linzhang Wang, and Jun Yang, "Exploit Imbalanced Cell Writes to Mitigate Write Disturbance in Dense Phase Change Memory", *The 52nd ACM/IEEE Design Automation Conference (DAC)*, 6 pages, June 2015. DOI: 10.1145/2744769.2744841

[11] Rujia Wang, Lei Jiang, Youtao Zhang, Linzhang Wang, and Jun Yang, "Selective Restore: an Energy Efficient Read Disturbance Mitigation Scheme for Future STT-MRAM", *The 52nd ACM/IEEE Design Automation Conference (DAC)*, 6 pages, June 2015. DOI:10.1145/2744769.2744908

[12] Xianwei Zhang, Youtao Zhang, and Jun Yang, "Adaptive Lane Borrowing of Hybrid Memory Cube", (Poster), *The 52nd ACM/IEEE Design Automation Conference (DAC)*, June 2015.

[13] Jiwei Liu, Jun Yang, and Rami Melhem, "GASOLIN: Global Arbitration for Streams of Data in Optical Links", 2015 IEEE International Parallel and Distributed Processing Symposium, pp.93-102, May 2015, doi:10.1109/IPDPS.2015.61.DOI: 10.1109/IPDPS.2015.61

[14] Yi Xu, Jun Yang, and Rami Melhem, "BandArb: Mitigating the Effects of Thermal and Process Variations in Silicon-Photonic Network", The 12th ACM International Conference on Computing Frontiers, pp. 30:1-30:8, May 2015, doi:10.1145/2742854.2742876. DOI:10.1145/2742854.2742876

[15] Xianwei Zhang, Youtao Zhang, Bruce Childers, and Jun Yang, "Exploiting DRAM Restore Time Variations in Deep Sub-micron Scaling", *Design, Automation and Test in Europe (DATE),* pp. 477-482, 2015.

[16] Lei Jiang, Bo Zhao, Jun Yang, and Youtao Zhang, "A Low Power and Reliable Charge Pump Design for Phase Change Memories," ***ACM/IEEE International Symposium on Computer Architecture (ISCA)***, pp. 397-408, June 2014.

[17] Lei Jiang, Youtao Zhang, and Jun Yang, "Mitigating Writes Disturbance in Super Dense Phase Change Memories," *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, pp. 216-227, June 2014.

[18] Xianwei Zhang, Lei Jiang, Youtao Zhang, Chuanjun Zhang, Jun Yang, "WoM-SET: Lowering Write Power of Proactive-SET based PCM Write Strategy Using WoM Code," *The International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 217-222, Sept. 2013. **Best Paper Award.** (citations: 6)

[19] Ping Zhou, Youtao Zhang, Jun Yang, "The Design of Sustainable Wireless Sensor Network Node using Solar Energy and Phase Change Memory," *Design, Automation and Test in Europe (DATE)*, interactive presentations, pp. 869-872, March 2013.

[20] Jie Guo, Jun Yang, Youtao Zhang, Yiran Chen, "Low Cost Power Failure Protection for MLC NAND Flash Storage Systems with PRAM/DRAM Hybrid Buffer," *Design, Automation and Test in Europe (DATE)*, pp. 859-864, March 2013.

[21] Bo Zhao, Youtao Zhang, Jun Yang, "A Speculative Arbiter Design to Enable High-Frequency Many-VC Router in NoCs,", *the 7th International Symposium on Networks-on-Chip*, pp. 1-8, DOI: 10.1109/NoCS.2013.6558415, April, 2013. (acceptance rate: 25%)

[22] Lei Jiang, Youtao Zhang, Bruce Childers, Jun Yang, "FPB: Fine-grained Power Budgeting to Improve Write Throughput of Multi-level Cell Phase Change Memory," ***the 45th IEEE/ACM International Symposium on Microarchitecture (MICRO)***, pp. 1-12, December 2012. (acceptance rate: 40/228=17.5%, citations: 25).

[23] Lei Jiang, Youtao Zhang, Jun Yang, "ER: Elastic RESET for Low Power and Long Endurance MLC Based Phase Change Memory," *International Symposium on Low Power Electronics and Design (ISLPED),* pp. 39-44, August, 2012. **Best Paper Nominee.** (acceptance rate: 17%, citations: 20)

[24] Yi Xu, Jun Yang, Rami Melhem, "Tolerating Process Variations in Nanophotonic On-chip Networks," ***the 39th International Symposium on Computer Architecture (ISCA)***, pp. 142-152, June 2012. (acceptance rate: 47/262=18%, citations: 17)

[25] Yi Xu, Jun Yang, Rami Melhem, "Channel Borrowing: An Energy-Efficient Nanophotonic Crossbar Architecture with Light-Weight Arbitration," *International Conference on Supercomputing (ICS),* pp. 133-142, June 2012. (acceptance rate: 36/161=22.3%)

[26] Lei Jiang, Bo Zhao, Youtao Zhang, Jun Yang, "Constructing Large and Fast Multi-Level Cell STT-MRAM Based Cache for Embedded Processors," *the 49th Design Automation Conference (DAC),* pp. 907-912, June 2012. (acceptance rate: 22%)

[27] Lei Jiang, Bo Zhao, Youtao Zhang, Jun Yang, Bruce Childers, "Improving Write Operations in MLC Phase Change Memory," ***the 18th International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 201-210, February, 2012. (acceptance rate: 17%, citations: 72)

[28] Bo Zhao, Jun Yang, Youtao Zhang, Yiran Chen, Hai Li, "Architecting a Common-Source-Line Array for Bipolar Non-Volatile Memory Devices," *Design, Automation and Test in Europe (DATE)*, interactive presentations, pp. 1451-1454, Mar. 2012. (acceptance rate: 27%)

[29] Lin Li, Youtao Zhang, Jun Yang, "Proactive Recovery for BTI in High-K SRAM Cells," *Design, Automation and Test in Europe (DATE)*, pp. 992-997, Mar. 2011. (acceptance rate: 34%)

[30] Lei Jiang, Yu Du, Youtao Zhang, Bruce Childers, Jun Yang, "LLS: Cooperative Integration of Wear-Leveling and Salvaging for PCM Main Memory," *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN),* pp. 221-232, June 2011. (acceptance rate: 26/148=18%)

[31] Yi Xu, Yu Du, Youtao Zhang, Jun Yang, "A Composite and Scalable Cache Coherence Protocol for Large Scale CMPs," *the 25th International Conference on Supercomputing (ICS),* pp. 285-294, May 2011. (acceptance rate: 22%)

[32] Lei Jiang, Youtao Zhang, Jun Yang, "Enhancing Phase Change Memory Lifetime Through Fine-Grained Current Regulation and Voltage Upscaling," *the International Symposium on Low Power Electronics and Design (ISLEPD),* pp. 127-132, August, 2011. (acceptance rate: 34%)

[33] Ping Zhou, Bo Zhao, Youtao Zhang, Jun Yang, Yiran Chen, "MRAC: A Memristor-Based Reconfigurable Framework for Adaptive Cache Replacement," *the 20th International Conference on Parallel Architecture and Compilation Techniques (PACT),* poster, pp. 207-208, October, 2011.

[34] Lin Li, Youtao Zhang, Jun Yang, Jianhua Zhao, "Proactive NBTI Mitigation for Busy Functional Units in Out-of-Order Microprocessors,'' *Design, Automation and Test in Europe (DATE)*, pp. 411-416, March, 2010. (acceptance rate: 30%)

[35] Yi Xu, Bo Zhao, Youtao Zhang, Jun Yang, ''Simple Virtual Channel Allocation for High Throughput and High Frequency On-chip Routers," ***the 16th International Symposium on High-Performance Computer Architecture (HPCA)***, 11 pages, January 2010. (acceptance rate: 18%, citations: 31)

[36] Ping Zhou, Yu Du, Youtao Zhang, Jun Yang, "Fine-grained QoS Scheduling for PCM-based Main Memory Systems," *the 24th IEEE International Symposium on Parallel and Distributed Processing (IPDPS),* 12 pages, April, 2010. (acceptance rate: 127/527=24%)

[37] Bo Zhao, Yu Du, Youtao Zhang, Jun Yang, "Variation-Tolerant Non-Uniform 3D Cache Management in Die Stacked Multicore Processor," ***the 42nd IEEE/ACM International Symposium on Microarchitecture (MICRO)***, pp. 222-231, December 2009. (acceptance rate: 25%, citations: 19)

[38] Ping Zhou, Bo Zhao, Jun Yang, Youtao Zhang, "Energy Reduction for STT-RAM Using Early Write Termination," *IEEE/ACM 2009 International Conference on Computer-Aided Design (ICCAD)*, pp. 264-268, November, 2009. (acceptance rate: 115/438=26%, citations: **156**)

[39] Ping Zhou, Bo Zhao, Jun Yang, Youtao Zhang, "A Durable and Energy Efficient Main Memory Using Phase Change Memory Technology," ***the 36th International Symposium on Computer Architecture (ISCA)***, pp. 14-23, June, 2009. (acceptance rate: 43/210=20%, citations: **476**)

[40] Yi Xu, Yu Du, Bo Zhao, Xiuyi Zhou, Youtao Zhang, Jun Yang, "A Low-Radix and Low-Diameter 3D Interconnection Network Design," ***the 15th International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 30-41, February 2009. (acceptance rate: 35/184=19%, citations: 76)

▶ **Best Paper Award Nominee**

[41] Ping Zhou, Bo Zhao, Yi Xu, Yu Du, Youtao Zhang, Jun Yang, Li Zhao, "Frequent Value Compression in Packet-based NoC Architectures," *the 14th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 13-18, January 2009. (acceptance rate: 116/355=33%)

[42] Xiuyi Zhou, Yi Xu, Yu Du, Youtao Zhang, Jun Yang, "Thermal Management for 3D Processors via Task Scheduling," *the 37th International Conference on Parallel Processing(ICPP)*, pp. 115-122, September, 2008. (acceptance rate: 81/263=30%, citations: 50)

[43] Jun Yang, Xiuyi Zhou, Marek Chrobak, Youtao Zhang, Lingling Jin, "Dynamic Thermal Management through Task Scheduling," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 191-201, April, 2008. (acceptance rate: 22/63=35%, citations: **111**)

[44] Wei Wu, Jun Yang, Sheldon X.-D. Tan, Shih-Lien Lu, "Improving the Reliability of On-Chip Caches Under Process Variations," *IEEE International Conference on Computer Design (ICCD)*, pp. 325-332, October 2007. (acceptance rate: 88/259=33%)

▶ **Best Paper Award (processor architecture track)**

[45] Jia Yu, Jinnan Yao, Laxmi Bhuyan, Jun Yang, "Program Mapping for Network Processors by Recursive Bipartitioning and Refining," *the 44th IEEE/ACM Design Automation Conference (DAC)*, pp. 805-810, June 2007. (acceptance rate: 161/713=23%)

[46] Weijia Li, Youtao Zhang, Jun Yang, Jiang Zheng, "UCC: Update-conscious Compilation for Energy-efficiency in Wireless Sensor Networks," ***ACM SIGPLAN Conference on Programming***

Language Design and Implementation (PLDI), pp. 383-393, June 2007. (acceptance rate: 45/178 =25%, citations: 27)

[47] Weijia Li, Youtao Zhang, Jun Yang, "Dynamic Authentication-key Reassignment for Reliable Report Delivery," *IEEE 3rd International Conference on Mobile Ad-hoc and Sensor Systems*, pp. 467-476, October 2006. (acceptance rate: 24%)

[48] Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang, Youtao Zhang, "Reduce Register File Leakage through Cell Discharging," *IEEE International Conference on Computer Design (ICCD)*, October 2006. (acceptance rate: 31%)

[49] Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, Hsien-Hsin Lee, "A Low-cost Memory Remapping Scheme for Address Bus Protection," t*he 15th IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 74-83, 2006. (acceptance rate: 26%)

[50] Wei Wu, Lingling Jin, Jun Yang, Pu Liu, Sheldon X.-D. Tan, "A Systematic Method for Functional Unit Power Estimation in Microprocessors," *the 43th IEEE/ACM Design Automation Conference (DAC)*, pp. 554-557, 2006. (acceptance rate: 209/865=24%, citations: 61)

[51] Youtao Zhang, Jun Yang, Lingling Jin, Weijia Li, "Locating Compromised Sensor Nodes through Incremental Hashing Authentication," *IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS)*, pp. 321-337, 2006. (acceptance rate: 30%)

[52] Youtao Zhang, Jun Yang, Hai Vu, "Interleaved Authentication for Filtering False Reports in Multipath Routing Based Sensor Networks," *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, April 2006. (acceptance rate: 23%)

[53] Weidong Shi, Josh Fryman, Hsien-Hsin Lee, Youtao Zhang, Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory," ***the 12th IEEE International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 225-234, February 2006. (acceptance rate: 14%, citations: 35)

[54] Lingling Jin, Wei Wu, Jun Yang, Chuanjun Zhang, Youtao Zhang, "Dynamic Co-allocation of Level One Caches," *the 2nd International Conference on Embedded Software and Systems*, pp. 373-385, December 2005.

[55] Jia Yu, Jun Yang, Shaojie Chen, Yan Luo, Laxmi Bhuyan, "Enhancing Network Processor Simulation Speed with Statistical Input Sampling," *2005 International Conference on High Performance Embedded Architectures & Compilers (HiPEAC)*, LNCS, Vol. 3793, pp. 68-83, 2005. (acceptance rate: 18%)

[56] Pu Liu, Zhenyu Qi, Hang Li, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Fast Thermal Simulation for Architecture Level Dynamic Thermal Management," *IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 638-643, 2005. (acceptance rate: 25%)

[57] Hang Li, Pu Liu, Zhenyu Qi, Lingling Jin, Wei Wu, Sheldon X.-D. Tan, Jun Yang, "Efficient Thermal Simulation for Run-Time Temperature Tracking and Management," *IEEE International Conference on Computer Design (ICCD)*, pp. 130-133, 2005. (acceptance rate: 101/313=32%)

[58] Dinesh Suresh, Banit Agrawal, Walid Najjar, Jun Yang, "VALVE: Variable Length Value Encoding for Off-Chip Data Busses," *IEEE International Conference on Computer Design (ICCD)*, pp. 631-633, 2005. (acceptance rate: 101/313=32%)

[59] Dinesh Suresh, Banit Agrawal, Walid Najjar, Jun Yang, "Tunable Bus Encoder for off-Chip Data Buses," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 319-322, August 2005. (acceptance rate: 72/233=31%)

[60] Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, "Low Power Network Processor Design Using Clock Gating," *the 42nd IEEE/ACM Design Automation Conference (DAC)*, pp. 712-715, June 2005. (acceptance rate: 154/735=20%)

[61] Yongjing Lin, Youtao Zhang, Quanzhong Li, Jun Yang, "Supporting Efficient Query Processing on Compressed XML Files," *the 20th ACM Annual Symposium on Applied Computing (SAC)*, pp. 660-665, March 2005. (acceptance rate: 278/764=36%)

[62] Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Automatic Design Exploration of DVS in Network Processor Architectures," *Design, Automation & Text in Europe (DATE)*, pp. 92-97, vol. 1, March 2005. (acceptance rate: 176/825=21%)

[63] Youtao Zhang, Lan Gao, Jun Yang, Xiangyu Zhang, Rajiv Gupta, "SENSS: Security Enhancement to Symmetric Shared Memory Multiprocessors," ***the 11th IEEE International Symposium on High-Performance Computer Architecture (HPCA)***, pp. 352-362, February 2005. (acceptance rate: 15%, citations: 61)

[64] Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar, "A Way-Halting Cache for Low-Energy High Performance Systems," *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 126-131, August 2004. (acceptance rate: 70/204=34%)

[65] Chuanjun Zhang, Jun Yang, Frank Vahid, "Low Static-Power Frequent-Value Data Caches," *Design, Automation & Text in Europe (DATE)*, pp. 214-219, February 2004. (acceptance rate: 23%)

[66] Dinesh Suresh, Banit Agrawal, Jun Yang, Walid Najjar, Laxmi Bhuyan, "Power Efficient Encoding Techniques for Off-chip Data Buses," *ACM International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, pp. 267-275, October 2003. (acceptance rate: 31/162=19%)

[67] Jun Yang, Youtao Zhang, Lan Gao, "Fast Secure Processors for Inhibiting Software Privacy and Tampering," ***ACM/IEEE 36th International Symposium on Microarchitecture (MICRO)***, pp. 351-360, December 2003. (acceptance rate: 35/134=26%, citations: **139**)

[68] Dinesh Suresh, Jun Yang, Chuanjun Zhang, Banit Agrawal, Walid Najjar, "FV-MSB: A Scheme for Reducing Transition Activity on Data Bus," *the 10th Annual International Conference on High Performance Computing (HiPC)*, pp. 44-54, December 2003. (acceptance rate: 48/164=29%)

[69] Youtao Zhang, Jun Yang, "Procedural Level Address Offset Assignment of DSP Applications with Loops," *IEEE International Conference on Parallel Processing (ICPP)*, pp. 21-28, October 2003.

[70] Jun Yang, Jia Yu, Youtao Zhang, "Lightweight Set Buffer: Low Power Data Cache for Multimedia Applications," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 270-273, August 2003. (acceptance rate: 90/221=41%)

[71] Youtao Zhang, Jun Yang, "Low Cost Instruction Cache Design for Tag Comparison Elimination," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 266-269, August 2003. (acceptance rate: 90/221=41%)

[72] Jun Yang, Rajiv Gupta, "Energy Efficient Frequent Value Data Cache Design," ***ACM/IEEE the 35th International Symposium on Microarchitecture (MICRO)***, pp. 197-207, November 2002. (acceptance rate: 36/150=24%, citations: **97**)

[73] Jun Yang, Rajiv Gupta, "FV Encoding for Low-Power Data I/O," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 84-87, August 2001. (acceptance rate: 73/194=38%, **22** citations)

[74] Jun Yang, Rajiv Gupta, "Energy-Efficient Load and Store Reuse," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 72-75, August 2001. (acceptance rate: 73/194=38%)

[75] Jun Yang, Youtao Zhang, Rajiv Gupta, "Frequent Value Compression in Data Caches," ***ACM/IEEE the 33rd International Symposium on Microarchitecture (MICRO)***, pp. 258-265, December 2000. (acceptance rate: 31/110=28%, citations: **150**)

[76] Youtao Zhang, Jun Yang, Rajiv Gupta, "Frequent Value Locality and Value-Centric Data Cache Design," ***ACM 9th International Conference on Architecture Support for Programming Lan-***

guages and Operating Systems (ASPLOS), pp. 150-159, November 2000. (acceptance rate: 24/114=21%, citations: **157**)

[77] Jun Yang, Rajiv Gupta, "Load Redundancy Removal through Instruction Reuse," *IEEE International Conference on Parallel Processing (ICPP)*, pp. 61-68, August 2000.

REFEREED WORKSHOP PUBLICATIONS

[1] Lin Li, Xiuyi Zhou, Jun Yang, Victor Puchkarev, "ThresHot: An Aggressive Task Scheduling Approach in CMP Thermal Design", *Workshop on Unique Chips and Systems, in conjunction with ISPASS2009*, April, 2009.

[2] Jia Yu, Wei Wu, Xi Chen, Harry Hsieh, Jun Yang, F. Balarin, "Assertion-Based Power/ Performance Analysis of Network Processor Architectures," *IEEE International High Level Design Validation and Test Workshop*, November 2004.

[3] Youtao Zhang, Jun Yang, Yongjing Lin, Lan Gao, "Architectural Support for Protecting User Privacy on Trusted Processors," *The Workshop on Architectural Support for Security and Anti-Virus, in conjunction with the 11th ASPLOS*, pp. 114-119, October 2004.

TEACHING EXPERIENCE

New Course Developed

ECE 3162 Advanced Computer Microarchitecture (Spring 2012, University of Pittsburgh)

This research-oriented course was designed for Ph.D. students. It is an in-depth exploration of important key issues in computer architecture in the era of nanometer technology and may-core integration. The students will be exposed the state-of-the-art research challenges and opportunities when looking into the next generation computer architecture. The main topics covered in the class are: 1. emerging technologies in memory system design such as Phase Change Memories, STT-RAM, and NAND flash memories; 2. massively parallel microprocessors such as Graphics Processing Units; 3. hardware reliability and yield issues including transient errors, hard errors, error diction and recovery; 4. programmability of parallel computing platforms (such as multicore architecture) including the cache consistency models and the new concepts of transactional memory. Students are exposed to the forefront of research advancement. They are also involved in research projects that are expected to result in near-future publications.

ECE 2162 Computer Architecture (Spring 2007, University of Pittsburgh)

This course was fully upgraded to focus on the latest developments in microarchitecture. Apart from techniques in the textbook, students were exposed to design details of commercial high-end microprocessors such as Core i7 from Intel. In addition, major research infrastructures such as Simplescalar and Simics were introduced in classroom and students were requested to use them in exercises. Extensive programming projects on instruction scheduling, out-of-order execution, and superscalar pipeline were developed for students to learn the in-depth designs of real processors. Research articles were also incorporated as course material and extra readings for students.

ECE 2195 Modern Computer Processor and System Architecture (Fall 2007, University of Pittsburgh)

Dr. Yang developed this new course for senior level graduate students to broaden their view in computer architecture. This course covers the most up-to-date technologies in planar multi-core and 3D chip architecture. The latest research articles were extensively discussed as the main course material. Dr. Yang designed new projects that cover the important aspects such as power and thermal management, interconnection network and cache management in CMP and 3D chips. Students were

trained with the widely used research tools such as Simics, Simplescalar, HotSpot, Orion, Cacti. Circuit level designs were also heavily incorporated in the projects.

CSE 260 Computer Architecture Seminar (Winter 2003, Spring 2005, University of California Riverside)

This course was offered once every two years, with a goal to cover the latest technologies developed in the last two years. In the first offer in 2003, Dr. Yang developed a syllabus that incorporated low power techniques in cache memories, buses; frequent value compression and encoding (Dr. Yang's thesis research); simultaneous multithreading technique; and network processor architectures. Dr. Yang designed a set of projects related to the above lectured topics. Most of the projects resulted in conference and journal publications. The network processor project later developed into a Ph.D. thesis topic for Dr. Yan Luo. In the 2005 offering, Dr. Yang developed material that covers in-depth design details of secure processors, memory protection and information flow tracking. The students were asked to simulate and evaluate the impact of various memory encryption/decryption and authentications schemes on the performance of a program.

CSE162 Computer Architecture (Spring 2006, University of California Riverside)

This course was developed to bridge the gap between its prerequisite CSE161 which covers the fundamentals in computer organization, and the entry level graduate computer architecture course CSE203A which covers more advanced material in computer architecture. This course was designed to include the data path and control path of pipelined architecture, including pipeline stall, forwarding, and flush; memory management including paging and virtual memory; multiprocessors and interconnection topologies; I/O systems; and network designs.

University of Pittsburgh

ECE 2162	Computer Architecture	Fall 2015	Enrollment:27
ECE 2162	Computer Architecture	Fall 2014	Enrollment:9
ECE 3162	Advanced Computer Microarchitecture	Spring 2014	Enrollment: 3
ECE 142	Computer Organization	Spring 2014	Enrollment: 50
ECE 2162	Computer Architecture	Fall 2013	Enrollment: 44
ECE 3162	Advanced Computer Microarchitecture	Spring 2013	Enrollment: 9
ECE 142	Computer Organization	Spring 2013	Enrollment: 47
ECE 3162	Advanced Computer Microarchitecture	Spring 2012	Enrollment: 5
ECE 2162	Computer Architecture	Fall 2011	Enrollment: 26
CoE/ECE 0142	Computer Organization	Spring 2011	Enrollment: 76
CoE/ECE 0142	Computer Organization	Spring 2010	Enrollment: 48
CoE/ECE 1896	Senior Design Project	Spring 2010	Enrollment: 15
ECE 2162	Computer Architecture	Fall 2009	Enrollment: 8
CoE/ECE 1896	Senior Design Project (undergraduate level)	Fall 2009	Enrollment: 28
ECE 2195	Modern Computer Processor and System Architecture (advanced graduate level)	Spring 2009	Enrollment: 9
ECE 2162	Computer Architecture	Fall 2008	Enrollment: 10
CoE/ECE 0142	Computer Organization	Spring 2008	Enrollment: 35

	(undergraduate level)		
ECE 2195	Modern Computer Processor and System Architecture (advanced graduate level)	Fall 2007	Enrollment: 11
ECE 2162	Computer Architecture (introductory graduate level)	Spring 2007	Enrollment: 19
CoE/ECE 0142	Computer Organization (undergraduate level)	Fall 2006	Enrollment: 20

University of California Riverside

CSE162	Computer Architecture (undergraduate level)	Spring 2006	Enrollment: 10
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2006	Enrollment: 21
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Fall 2005	Enrollment: 34
CSE260	Computer Architecture Seminar (advanced graduate level)	Spring 2005	Enrollment: 4
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2005	Enrollment: 16
CSE203A	Computer Architecture (introductory graduate level)	Fall 2004	Enrollment: 33
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Spring 2004	Enrollment: 63
CSE161	Design and Architecture of Computer Systems (undergraduate level)	Winter 2004	Enrollment: 60
CSE203A	Computer Architecture (introductory graduate level)	Fall 2003	Enrollment: 42
CSE260	Computer Architecture Seminar (advanced graduate level)	Winter 2003	Enrollment: 12
CSE203A	Computer Architecture (introductory graduate level)	Fall 2002	Enrollment: 28

PROFESSIONAL SERVICE ACTIVITIES

Editorial Board

1. Associate Editor – IEEE Computer Architecture Letters.

Conference/Workshop Organization Committee

1. Registration Chair – The fifth ACM/IEEE International Symposium on Networks-on-Chip, Pittsburgh, PA, May, 2011.

2. Finance and Registration Chair – Sixteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'11), Newport Beach, CA, Mar. 2011.
3. Finance and Registration Chair – Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'10), Pittsburgh, PA, Mar. 2010.
4. Finance and Registration Chair – IEEE Computer Society Annual Symposium on VLSI, 2009, Tampa, FL, May 2009.
5. Workshop/Tutorials Chair – 2009 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Boston, MA, Apr. 2009.
6. Program Chair − The 12th Workshop on Interaction between Compilers and Computer Architecture (Interact-12), in conjunction with the 14th International Symposium on High-Performance Computer Architecture (HPCA14), Salt Lake City, Utah, Feb. 2008.
7. Program Chair − The 16th International Conference on Computer Communications and Networks, Computer Architecture for Networking and Communications Track, Honolulu, Hawaii, Aug. 2007.
8. Program Chair − The International Conference on Embedded and Ubiquitous Computing (EUC), Embedded System Architecture Track, Seoul, Korea, Aug. 2006.

Technical Program Committee Member

1. The 19th and 20th IEEE International Symposium on High Performance Computer Architecture (HPCA), 2013, 2014, 2016.
2. Design Automation Conference (DAC), June 2015
3. The 29th IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 2015
4. International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES), Oct., 2015
5. The 32nd IEEE International Conference on Computer Design (ICCD), October 2014, 2015
6. The Memory Forum 2014, in conjunction with ISCA 2014, June 2014.
7. The 42nd Annual Conference on Parallel Processing (ICPP), October 2013, 2015.
8. The 6th, 7th ACM/IEEE International Symposium on Networks-on-Chip (NOCS), 2012-2015.
9. 2011 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, TX, Apr. 2011.
10. 21st International Symposium on Computer Architecture and High Performance Computing, computer architecture track, Sao Paulo, Brazil, Oct. 2009.
11. The 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects, in conjunction with 36th International Symposium on Computer Architecture (ISCA), Austin, TX, Jun. 2009.
12. Workshop on Unique Chips and Systems (UCAS-5), in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2009, Boston, MA, Apr. 2009.
13. International Symposium on Low Power Electronics and Design (ISLPED), Bangalore, India, Aug. 2008.
14. The 13th Asia and South Pacific Design Automation Conference (ASP-DAC), Student Forum, Jan. 2008.
15. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 35th International Symposium on Computer Architecture (ISCA), Beijing, China, Jun. 2008.
16. The 14th IEEE International Conference on High Performance Computing (HiPC), Goa, India, Dec. 2007.
17. International Symposium on Low Power Electronics and Design (ISLPED), Portland, Oregon, Aug. 2007.

18. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 34th International Symposium on Computer Architecture (ISCA), San Diego, California, Jun. 2007.
19. The 2nd International Conference on Embedded Software and Systems, Xian, China, Dec. 2005.
20. ACM SIGPLAN/SIGBED 2005 Conference on Language, Compilers, and Tools for Embedded Systems (LCTES), Jun. 2005.
21. The 10th IEEE International Conference on High Performance Computing (HiPC), Hyderabad, India, Dec. 2003.

NSF Panelist

1. NSF panelist: Large projects ($1.2M -- $3M), March 2015
2. NSF Foundations of Computing Processes and Artifacts Cluster, March 2008
3. NSF CAREER, October 2008
4. NSF CAREER, October 2009
5. NSF Cyber Trust, April 2005

Conference/Workshop Session Chair

1. IEEE International Symposium on High Performance Computer Architecture, February 2014
2. International Symposium on Performance Analysis of Systems and Software, April 2008
3. Workshop on the Interaction between Operating Systems and Computer Architecture, in conjunction with the 35th International Symposium on Computer Architecture (ISCA), Beijing, China, Jun. 2008
4. ACM/IEEE International Symposium on Low Power Electronics and Design, August 2007

Reviewer for

IEEE Transactions on Computers, 2000 – 2015
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2005 – 2015
IEEE Transactions on Very Large Scale Integrated Systems 2005 – 2015
IEEE Transactions on Parallel and Distributed Systems 2007
IEEE MICRO 2002 – 2009
IEEE Computer Architecture Letters 2005 – 2014
ACM (Association of Computing Machinery) Transactions on Design Automation of Electronic Systems 2002 – 2015
ACM Transactions on Architecture and Code Optimization 2002 – 2015
ACM Transactions on Embedded Computing Systems 2002 – 2008
Elsevier Journal of Computer Languages, Systems & Structures 2007
Journal of VLSI Signal Processing Systems 2006
International Symposium on Computer Architecture (ISCA) 2006 – 2014
International Symposium on Microarchitecture (MICRO) 2001 – 2014
International Symposium on High Performance Computer Architecture (HPCA) 2008-2016
ACM SIGPLAN Conference on Program Language Design and Implementation (PLDI) 2004
International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES) 2004 – 2015
Design, Automation & Test in Europe (DATE) 2004 – 2006
International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS) 2003 – 2004

INVITED PRESENTATIONS

1. "Making A Way to An Academic Career", IEEE Women in Engineering, International Conference on Computer Design, Oct. 2015.

2. "Towards A Competitive Dense Phase Change Memory", University of Central Florida, Jan. 2015.
3. "WoM-SET: Lowering Write Power of Proactive-SET based PCM Write Strategy Using WoM Code," International Symposium on Low Power Electronics and Design, Beijing, China, Sept. 2013.
4. "Frequent Value Compression in Packet-based NoC Architectures," given at the 14th Asia and South Pacific Design Automation Conference, Yokohama, Japan, January 2009.
5. "A Low-Radix and Low-Diameter 3D Interconnection Network Design," given at the Computer Science and Technology Department, Nanjing University, Nanjing, China, December, 2008.
6. "A Low-Radix and Low-Diameter 3D Interconnection Network Design," given at the Computer Architecture Lab at Carnegie Mellon (CALCM), ECE Department, Carnegie Mellon University, November, 2008.
7. "Dynamic Thermal Management through Task Scheduling," given at the 2008 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, TX, Apr. 2008.
8. "Dynamic Thermal Monitoring and Management for High-Performance Microprocessor," given at the Intel Research Lab, Pittsburgh, Feb. 2007.
9. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the Intel Asia-Pacific Research Development, Ltd. Shanghai, China, Dec. 2006.
10. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the School of Microelectronics, Shanghai Jiaotong University, Shanghai, China, Dec. 2006.
11. "Dynamic Power and Thermal Monitoring for High-Performance Microprocessors," given at the Computer Science Department, University of Pittsburgh, Dec. 2006.
12. "Dynamic Power and Thermal Monitoring for High-Performance Microprocessors," given at the Department of Computer Science and Engineering, Pennsylvania State University, Oct. 2006.
13. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of California Riverside, May, 2002.
14. "Frequent Value Phenomenon and its Applications,", given at the Department of Computer Science and Engineering, University of Texas Arlington, Apr. 2002..
15. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of North Texas, Apr. 2002.
16. "Frequent Value Phenomenon and its Applications," given at the Computer Science Department, Rutgers, the State University of New Jersey, Apr. 2002.
17. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science, State University of New York Binghamton, Apr. 2002.
18. "Frequent Value Phenomenon and its Applications," given at the Department of Computer Science and Engineering, University of Connecticut, Mar. 2002.
19. "Frequent Value Phenomenon and its Applications," given at the Department of Computer and Information Sciences, University of Delaware, Mar. 2002.
20. "FV Encoding for Low-Power Data I/O," given at the ACM/IEEE International Symposium on Low Power Electronics and Design, Huntington Beach, CA, Aug. 2001.
21. "Energy-Efficient Load and Store Reuse," given at the ACM/IEEE International Symposium on Low Power Electronics and Design, Huntington Beach, CA, Aug. 2001.
22. "Frequent Value Compression in Data Caches," given at the ACM/IEEE 33rd International Symposium on Microarchitecture, Monterey, CA, Dec. 2000.
23. "Load Redundancy Removal through Instruction Reuse," given at the International Conference on parallel Processing, Toronto, Canada, Aug. 2000.

Internal Presentations

1. "Architectural Design and Consideration for 3D Chip Multiprocessors," given at the ECE Department Undergraduate Seminar, Sept. 2006.
2. "Dynamic Power and Thermal Monitoring and Managements for High-Performance Microprocessors," given at the ECE Department Graduate Seminar, Oct. 2006.
3. "Towards an Energy and Thermally Efficient High-Performance Microprocessor Design," given at the ECE Department Undergraduate Seminar, Nov. 2006.
4. "Low Power and Thermal Management for High-Performance Microprocessor Designs," given at the IEEE Chapter, Undergraduate Seminar ECE Department, Nov. 2006.

DEPARTMENTAL ADMINISTRATIVE ACTIVITIES

COMMITTEES

1. Graduate committee, ECE Dept. of Pittsburgh, 2009-2013.
2. Faculty recruiting committee, ECE Dept. University of Pittsburgh, 2008-2012, 2014.
3. Graduate admission, computer engineering area, ECE Dept., University of Pittsburgh, 2006-2014.
4. Graduate admission committee, Dept. of Computer Science and Engineering, University of California Riverside, 2005 – 2006.
5. Faculty recruiting committee, Dept. of Computer Science and Engineering, University of California Riverside, 2003 – 2005.

DISSERTATION/THESIS COMMITTEE

University of Pittsburgh: Gerold Joseph (MS), Colin Ihrig (MS and PhD), Gayatri Mehta (PhD), Justin Stander (MS), Ruibin Xu (PhD), Mohammad Hammoud (PhD), Taecheol Oh (PhD), Hunjin Lee (PhD), Jeff Vance (MS), Peiyuan Wang (MS), Xiang Chen (PhD), Zhenyu Sun (PhD), Juyoung Jung (PhD), Santiago Bock (PhD), David Dgien (MS), Nathan Altay Hunter (MS)

University of California Riverside: Jinnan Yao (PhD), Jiani Guo (PhD), Dinesh Suresh (PhD), Li Zhao (PhD), Susan Lysecky (PhD), Roman Lysecky (PhD), Ann Gordon-Ross (PhD), Greg Stitt (PhD), Chuanjun Zhang (PhD), Xi Chen (PhD), Jessica Lin (PhD), Chotirat (Ann) Ratanamahatana (PhD), Xiaopeng Xi (PhD), Junjie Yang (PhD)

Georgia Institute of Technology: Tao Zhang (PhD) – external member

College of William and Mary: Zhichun Zhu (PhD) – external member

City University of Hong Kong: Yazhi Huang (PhD), Qingan Li (PhD) – external member